ABSTRACT

Circuits, devices and methods are provided for dividing a fast pulse signal by an integer M. A dual modulus prescaler receives input pulses, counts them, and generates one prescaled pulse for every Qth input pulse. Q is a division modulus, and has a different value depending on a modulus control signal. When the prescaler generates a prescaled pulse from an input pulse, it ignores the modulus control signal at least until the onset of a next input pulse. A program counter generates a reset signal when the prescaler receives the Mth input pulse. A swallow counter then changes the modulus control signal to a different value, and the prescaler starts dividing by a different modulus. Even if the prescaler had already received the onset of the next input pulse, it accounts for it properly, for dividing with the different modulus.